## REMARKS

The allowance of claims 72-74 and 81-83 is gratefully acknowledged by the Applicant. The statement by the Examiner that claims 66-69 and 78-80 contain allowable subject matter is also gratefully acknowledged.

Claims 63 and 75 have been amended solely to clarify the recited inputs and not for purposes of patentability or in response to rejection. The Application contains claims 63-83, of which claims 72-74 and 81-83 have been allowed. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 63-65, 70, 71 and 75-77 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Takahashi et al., U.S. Patent No. 5,528,545 (hereinafter "Takahashi"). The rejection is respectfully traversed.

Claim 63 recites a static memory device comprising "a static memory cell connected to first and second bit lines; an input circuit having first and second inputs for inputting data to be written into a memory cell; and a current generating circuit for generating first and second currents in response to received input data and applying the first and second currents to the memory cell through the bit lines." According to claim 63, "said first and second currents represent[] a value of the input data."

Applicant respectfully submits that Takahashi relates solely to sense amplifiers for sensing the values stored in a memory cell. Takahashi Col. 1, ll. 6-12, Col. 5, ll. 55-59, Col. 6, ll. 6-44. The main objective of Takahashi is to "read precisely a binary signal of a memory cell even if there is an offset current between a bit line pair." Takahashi Col. 5, ll. 55-59, see also Col. 9, l. 55 to Col. 10, lime 36 ("Therefore, by using sense amplifier SA10 of this embodiment, data stored in a memory cell can be sensed at a high speed . . ."). There is no disclosure whatsoever in Takahashi that relates to

writing values of input data into a memory cell, let alone writing into the cell by applying first and second currents (corresponding to the values of the input data) via the bit lines connected to the cell.

As such, claim 63 is allowable over Takahashi. Claims 64-65 and 70-71 depend from claim 63 and are allowable along with claim 63 for at least the reasons set forth above and on their own merits.

Claim 75 similarly recites "a current generating circuit for generating first and second currents in response to received input data and applying the first and second currents to the memory cell through the bit lines, said first and second currents representing a value of the input data." As set forth above, Applicant respectfully submits that Takahashi fails to disclose the invention of claim 75 since Takahashi fails to disclose writing values of input data into a memory cell by applying first and second currents (corresponding to the values of the input data) to the cell via the bit lines connected to the cell.

As such, claim 75 is allowable over Takahashi. Claims 76 and 77 depend from claim 75 and are allowable along with claim 75 for at least the reasons set forth above and on their own merits.

Applicant respectfully submits that the rejection be withdrawn and claims 63-65, 70, 71 and 75-77 be allowed.

Claims 66-69 and 78-80 stand objected to as being dependent upon rejected base claims, but are otherwise allowable. The objection is respectfully traversed and reconsideration is respectfully requested. Claim 66 depends from claims 65 and 63, claims 67-69 depend from claim 63, claim 78 depends from claims 77 and 75, and claims 78-80 depend from claim 75. As set forth above, Applicant respectfully submits that

claims 63, 65, 75 and 77 are allowable. Accordingly, claims 66-69 and 78-80 depend from allowable claims. The objection should be withdrawn and claims 66-69 and 78-80 allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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